Circuit Topology Optimization Using Logical Effort Technique

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Abstract

The logical effort method is one of the easiest ways to estimate delay in a CMOS circuit. The fastest logic structure can be nominated by comparing delay estimates of different logic circuits. This method helps to specify the appropriate number of logic gates on a path and the best transistor sizes for the logic gates. Since the method is easy to use, it is an epitome for weighing alternatives at the first stage of a design and offers a good starting point for more complex optimizations. In this research, the logical effort technique is applied on conventional circuit such as 2x1 multiplexer with two different circuits.

Keywords: Logical effort, Transistor sizing, Static CMOS circuit.